Exhibit S

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORP.
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION UNDER 37 C.F.R. § 41.77(f)

STATEMENT OF THE CASE

These proceedings involve U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon.

In our earlier Decision ("Dec.") mailed May 31, 2016, we affirmed the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi[1] under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC[2] under § 103, (4) claims 16 and 17 based on Amidi and Dell 2[3] under § 103, and (5) claims 57,[4] 58, 60, 68, 79, 84, 89–91, and 128–131 under § 112, first paragraph, as lacking written description support. Dec. 101–02. We additionally reversed the Examiner's decision not to adopt the rejections of:

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[1] U.S. Publ. 2006/0117152 A1 (published June 1, 2006 and filed Jan. 5, 2004) (Amidi).

[2] JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C); *JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C* (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C); *JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A)* 1-12 (May 2003) (JEDEC 82-4B). As indicated in the previous Decision, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

[3] U.S. Patent No. 6,209,074 (issued Mar. 27, 2001) (Dell 2).

[4] The summary at the end of the Decision (Dec. 102) mistakenly omits independent claim 57. *See id.* at 84–89 (discussing claim 57 under the Lack of Written Description Support section).

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136 based on Amidi and Dell 2 (Ground 5[5]) (*see id.* at 78–83, 102), (2) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on Micron[6] and Amidi (Ground 13) (*see id.* at 93–99, 102), (3) claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 based on Amidi and Dell 184[7] (Ground 20) (*see id.* at 91–93, 102), and (4) claims 52–54, 67–71, 77–79, 82–84, and 87–89 based on Micron, Amidi, and Olarig[8] (Ground 21) (*see id.* at 99–102). We designated the reversed, non-adopted rejections as new grounds. *Id.* at 102.

In Patent Owner's Response Requesting to Reopen Prosecution submitted August 1, 2016 (PO Response), Patent Owner canceled claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–130 of the '912 patent. PO Response 2. Previously, claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and 112–118 were canceled. *Id.* at 46. According to Patent Owner, claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–136 have been amended. *See id.* at 46. Patent Owner also submitted a declaration of Dr. Carl Sechen, dated July 31, 2016. Requesters 1 through 3 submitted comments (R1 Comments, R2 Comments, and R3 Comments) pursuant to 37 C.F.R. § 41.77(c) on August 31, 2016. Requester 1 presents a declaration of Dr. David Wang, dated August 30, 2016; Requester 2

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[5] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters refer to the various rejections by ground number. *See, e.g.*, RAN 11–15. We include the ground number here and throughout the Decision.
[6] Micron, *DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB* I-20 (2002) (Micron).
[7] U.S. Patent No. 6,446,184 B2 (issued Sept. 3, 2002) (Dell 184).
[8] U.S. Patent No. 6,260,127 B1 (issued July 10, 2001) (Olarig).

presents a declaration of Dr. Nader Bagherzadeh, dated August 31, 2016. Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 were the subject of the remand order mailed February 9, 2017. Order 5.[9]

On remand, the Examiner maintained the following rejections in the Examiner's Determination (Ex. Deter.):

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136[10] based on Amidi and Dell 2 (Ground 5),

(2) claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184 (Ground 20),

(3) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi (Ground 13), and

(4) claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig (Ground 21). Ex. Deter. 21.

The Examiner further adopted Requester 1's proposed rejection of (5) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C. *Id.*

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[9] A subsequent remand order was mailed May 2, 2017, and a Petition Decision related to the subsequent remand order was mailed June 5, 2017.

[10] The Examiner adds claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 to, and omits claims 120, 122 and 132–136 from, Ground 5. Ex. Deter. 21. We agree with Patent Owner that these additions and omissions were in error. PO Comments 2 n.1.

After the Examiner's Determination, Patent Owner submitted comments (PO Comments) on November 3, 2017 and Requester 1 responded (R1 Reply) on December 1, 2017 pursuant to 37 C.F.R. § 41.77(e).

This proceeding has returned to the Board under 37 C.F.R. § 41.77(f). Our new Decision is deemed to incorporate our earlier Decision, except for any portion specifically withdrawn. 37 C.F.R. § 41.77(f).

Claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 are independent claims; claim 58 depends from independent claim 57. Claim 57 was not part of the remand. The remaining claims on remand depend directly or indirectly from these claims. Illustrative, independent claim 1 reads as follows:

> 1. (Twice Amended) A memory module connectable to a computer system, the memory module comprising:
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> a printed circuit board;
>
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the

plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to *(i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal*.

PO Response 2–3 (underlining amendments relative to the originally issued claims and italicizing newly added subject matter relative to the claims as originally appealed).

The following summarizes various declarations in this proceeding:

Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),

Declaration of Dr. Carl Sechen dated July 31, 2016 (2d Supp.[11] Sechen Decl.),

Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

Declaration of Dr. David Wang dated August 30, 2016 (4th Wang Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 31, 2016 (4th[12] Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.), and

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.).

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[11] We deviate from our nomenclature for other declarations to be consistent with Patent Owner's discussion. *See, e.g.,* PO Response 47.

[12] Requester 2 describes this declaration as "Bagherzadeh Decl. V" (R2 Comments 8). We however number the declaration sequentially as part of this list.

Maintained/Adopted Rejections

In the Examiner's Determination, the Examiner maintains or adopts the following grounds of rejection:

References	Basis	Claims	Presented/Maintained
Amidi and Dell 2 (Ground 5)	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136	Dec. 78–83; Ex. Deter. 21; *see also* above footnote 10
Amidi, Dell 2, and JEDEC 21-C	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Ex. Deter. 21

Amidi and Dell 184 (Ground 20)	§ 103(a)	52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 91–93; Ex. Deter. 21
Micron and Amidi (Ground 13)	§ 103(a)	1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Dec. 93–99; Ex. Deter. 21
Micron, Amidi, and Olarig (Ground 21)	§ 103(a)	52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 99–102; Ex. Deter. 21

II. ISSUES

The main issues are whether Patent Owner has presented sufficient arguments and evidence to overcome the new grounds of rejection for and the newly adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 presented in the May 31, 2016 Decision and the Examiner's Determination.

III. ANALYSIS

A. Amidi and Dell 2 (Ground 5)

In our May 31, 2016 Decision, claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 (canceled claims omitted) were rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 78–83. Patent Owner presents several argument related to this ground, asserting the amendments to independent claims 1, 15, 28, and 39 overcome the new grounds. PO Response 50–53. Patent Owner asserts the claimed "logic element [now] generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal of the set of input control signals, and (iv) the PLL [phase lock loop] clock signal." *Id.* at 52; *see also id.* at 3 (underlining omitted). Throughout this Decision, we will refer to this new limitation as the "logic element" limitation and the response signals collectively as signals (i)–(iv) or individually as signal (i), (ii), (iii), or (iv).

Regarding the "logic element" limitation, Patent Owner argues (1) "Amidi's CPLD 604 never receives bank address signals," instead generating control signals (e.g., chip select signals rcs0a–rcs3b) based on a row address signal and chip-select signals and (2) Dell 2 does not cure Amidi's deficiencies. *Id.* at 52 (citing 2d Supp. Sechen Dec. ¶¶ 21–22, 25). Additionally, Patent Owner argues combining Amidi and Dell 2 would not teach or suggest to one skilled in the art generating control signals based on a row address signal and bank address signals as now recited in the claims. *See id.* at 52–53 (citing 2d Supp. Sechen Dec. ¶¶ 23–24, 26).

The Examiner maintained the Amidi/Dell 2 rejection on remand. Ex. Deter. 21. Citing to Requester 1–3's Comments, the Examiner determined the newly amended claim recitations, including the "logic element" limitation, have already been rejected in our previous Decision when addressing then existing claims 123, 128, and 129 (claims 128 and 129 are now canceled). *Id.* at 18 (citing R1 Comments 9, R2 Comments, and R3 Comments). Specifically, Requester 1 contends our previous Decision already determined Amidi and Dell 2 teach the recited "logic element" limitation. R1 Comments 7, 10–11 (citing 4th Wang Decl. ¶ 26 and Dec. 80–82, which refer to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach" (*id.* at 81)); *see also id.* at 40–43 (citing Amidi ¶ 71, Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, and 3d Bagherzadeh Decl. ¶ 37), 57–60 (citing Dell 2, 2:48–59, 8:36–41), 78–79 (citing Dell 2, 2:32–38). Requesters 2 and 3 present similar remarks. *See* R2 Comments 8–9 (discussing the similarities of the new claim amendments to claims 52, 123 (previously existed),[13] and 129 (now canceled)); *see also* R3 Comments 7–8 (discussing the previously existing claim 123).

We agree independent claim 52 and claim 123 (previously recited) included a recitation similar to the "logic element" limitation. For example, claim 52 previously recited "the logic element responds to at least a row address bit of the at least one row/column address signal, the bank address signals, and the at least one

[13] Requester 2 cites to "RAN Claims 42." R2 Comments 8. Requester 2 states "RAN Claims" refers to "Patent Owner Response/Amendment" submitted on January 14, 2013. *Id.* at 1. Because the amendment to claim 123 is located on page 38 (RAN Claims 38), we presume Requester 2 is referring to page 38 in the comments.

chip-select signal by generating a first number of chip-select signals of the set of output control signals." R1 App. Br., App'x A 17 (Claims App'x). Dependent claim 123 depends from claim 1 and previously recited "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals." *Id.*, App'x A 27 (Claims App'x). That is, other than the additional signal (iv) or the PLL clock signal now in claim 1 (PO Response 3), claim 1's "logic element" limitation generates chip-select signals in response to the same signals listed in previously recited claims 52 and 123.

However, when addressing Ground 5 (i.e., Amidi and Dell 2), we did not present a new ground of rejection for claim 52, 123, or 129. Dec. 78–83. Rather, we only presented a new ground of rejection for claims 52, 123, and 129 collectively based on Micron and Amidi (Ground 13). Dec. 93–99. As such, although these claims include similar subject matter to claim 1 as currently amended, we did not previously determine Amidi and Dell 2 teach or suggest the limitations found in claims 52, 123, and 129. Moreover, claim 1 previously recited the logic element "generates gated column access strobe (CAS) signals or chip-select signals . . . in response at least in part to a bank address signal" (R1 App. Br., App'x A 1) but did not recite that the CAS signals or chip-select signals were in response to bank address signal*s* as well as signals (i), (iii), and (iv) as now recited in claim 1.

For reasons discussed below and based on the record, we agree with Patent Owner that Amidi and Dell 2 would not teach or suggest to an ordinarily skilled

artisan the "logic element" limitation, which claims the logic element generates chip-select signals[14] in response to all four enumerated signals (i)–(iv) in claim 1.

In our previous decision, a register (e.g., 408) and a CPLD (e.g., 604) collectively were mapped to the recited "logic element." Dec. 18 (stating "we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited 'logic element.'") We analyzed whether Amidi taught or suggested a register (e.g., 408) receiving bank address signals. *See, e.g.,* Dec. 18–21, 27–34. As part of that analysis, we concluded Amidi at least suggests to an ordinarily skilled artisan some embodiments where signals other than those explicitly disclosed, including bank address signals, may be received by register 408. *See, e.g.,* Dec. 28, 30, 33.

However, as now claimed, claim 1 recites the logic element "generates chip-select signals" in response to signals (i)–(iv). In Amidi, its CPLD (e.g., 604 in Figures 6A-B)—not its registers—generates chip-select signals (e.g., rcs0a–3b). Amidi, Figs. 6A–B. Because Amidi's registers (e.g., 408, 418, and 608) do not teach or suggest "generat[ing] chip-select signals" (e.g., rcs0a–3b) and the signals Amidi's registers received do not attribute to the generated chip-select signals at Amidi's CPLD (*see* Amidi, Figs. 6A–B), Amidi's register (e.g., 408) can no longer be a component of claim 1's "logic element" limitation that generates the recited "chip-select signals" in response to signals (i)–(iv).

Amidi shows chip-select signals[15] (e.g., rcs0a–rcs3b) generated by CPLD 604 (e.g., a logic element). Amidi ¶¶ 52, 60, Figs. 6A–B. Also, Amidi teaches and

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[14] We discuss the alternatively generated, "gated column access strobe (CAS) signals" of claim 1 later in the Opinion.

[15] The '912 patent explains "rank-select signals" are "also called chip-select signals." The '912 patent 2:36–38.

shows a row address signal (e.g., Add(n) or signal (i)) and a chip-select signal (e.g., cs0 or cs1 or signal (iii)) are inputted into Amidi's CPLD 604. Amidi ¶¶ 49, 52, 58, 60, Fig. 6A. As such, Amidi generates chip-select signals in response to both signals (i) and (iii) in claim 1. But, as we previously found, Amidi "fails to describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD 410 or 604. *See* Amidi, Figs. 4A–B, 6A–B." Dec. 20; *see id.* at 36. Additionally, we agreed with Patent Owner that "Requester 1's proposed obviousness rejections based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a CPLD receiving BA signals." Dec. 39.

When discussing the obviousness rejection based on Amidi and Dell 2 (Ground 5), we stated "Amidi teaches emulating a smaller memory module by using an address signal, such as an extra row or column line, but does not specifically discuss using a bank address line." Dec. 79; *see id.* at 79–80 (referring to Grounds 4 and 6 for details). However, we additionally stated Dell 2's teaching "provide[s] some evidence of generating [] chip select or rank select signals in response at least in part to a bank address signal." Dec. 81 (referring to our discussion of "bank address limitation in claim 7"). Notably, the "bank address limitation in claim 7" addressed the previously recited "bank address signals of the set of input control signals are received by both the logic element and the register" (R1 App. Br., App'x A 4 (Claims App'x)), not the logic element generating chip-select signals in response to signals (i)–(iv) as claim 1 now recites (PO Response 3).

Even so, we stated "Amidi suggests other types of memory devices or densities can be used to build the four rank memory module" (Dec. 42 (citing Amidi ¶ 71)) and "Dell 2 teaches a technique for using various types of memory

devices or densities other than those in Amidi, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory device. Dell 2, Abstract, claim 1." *Id.; see also id.* at 42–43 (citing Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1). We also stated "the discussion of Amidi's CPLD receiving bank address signals . . . based on Dell 2's teaching as previously discussed, does provide some evidence of generating [] chip select or rank select signals in response at least in part to *a* bank address signal." *Id.* at 81 (italics added), *quoted in* R1 Comments 10; *see id.* at 94 (stating "Amidi . . . 'at least suggests generating a chip-select signal in response in part to *a* bank address signal'") (emphasis added), *quoted in* R3 Comments 11. These discussions do not address Amidi's and Dell 2 generating chip select signals in response to signals (ii) or "the bank address signal*s*" as now recited.

The previous Decision also states "Dell 2 provides a teaching or suggestion to direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1)." *Id.* at 81–82 and *see also* 4th Wang Decl. ¶ 26, *cited in* R1 Comments 11. Requester 2 also states Dell 2 discloses the bank address signals of the "logic element" limitation and one skilled in the art would have recognized generating a CAS or chip-select signal in response to a bank address signal in order to ensure the correct bank is addressed. R2 Comments 9–10 (citing 4th Bagherzadeh Decl. ¶ 10[16], which cites Dell 2, 8:29–44).

[16] Requester 2 provides no paragraph number. For purpose of this decision, we presume Requester 2 is referring to paragraph 10.

Specifically, Dell 2 teaches a logic circuit (e.g., a switch circuit) that performs a remapping function (e.g., 50) of at least one address signal (e.g., A12) to an additional bank address signal (e.g., BA1) at CAS time to ensure the correct *bank* is addressed. Dell 2, 2:32–37, 49–51, 8:20–40, Fig. 1A. Thus, based on Dell 2's teachings or suggestions and what one skilled in the art would have recognized, we agree with Requester 1 (R1 Comments 10–11), Dr. Wang (4th Wang Decl. ¶ 26), Requester 2 (R2 Comments 9–10), and Dr. Bagherzadeh (4th Bagherzadeh Decl. ¶ 10) that one skilled in the art would have recognized using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank* during bank expansion (e.g., generate *bank-select* signals in response to bank address signals).

Although this discussion addresses why bank address signals may be received by a CPLD, this reasoning does not sufficiently address why one skilled in the art would have recognized a CPLD, like Amidi's, (e.g., a logic element) generates *chip-select* signals in response to received bank address signals and the other recited signals (i.e., signals (i), (iii), and (iv) recited in claim 1. That is, having a logic element specifically generate "rank-selecting signals . . . in response to" bank address signals in combination with signals (i), (iii), and (iv) as now claim 1 presently recites does not follow from the above teaching to generate signals for *bank* selection. Nor does the current record sufficiently establish that one skilled in the art would have recognized applying Dell 2's bank expansion technique to Amidi's rank expansion process, such that the combination suggests the "logic element" limitation recited in claim 1. Moreover, even assuming, without deciding, one skilled in the art would have recognized to apply such a regime to Amidi's rank expansion process, the teachings would at best suggest

using one stored bank address signal—not bank address signals or signals (ii) required in claim 1—to generate chip-select signals.

The above-discussed teachings are inadequate to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal and bank address signal*s* as recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 25 (stating "[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal"), 26 (stating "[t]here is no suggestion to repurpose a bank address signal for rank multiplication purposes."). Thus, in view of the record as it currently stands, we have reconsidered and withdraw our statement in the previous Decision that combining Dell 2's teaching with Amidi "would have predictably yielded" the logic element receiving bank address signals "so that the necessary rank chip select signals discussed in Amidi are produced" (*id.* at 43) as well as any other similar statements.

We additionally referred to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach." *Id.* at 81; *see also id.* at 82 and R1 Comments 23 (citing Dec. 81–82). For example, we discussed Dell 2 teaches "storing signals for later use, including during a column access procedure[], to ensure the correct bank is addressed." Dec. 59; *see also id.* at 80. As explained above, this teaching in Dell 2 does not teach or suggest sufficiently to one skilled in the art a "logic element" limitation generating *chip-select* signals in response to both a row address signal (i.e., signal (i)) and bank address signal*s* (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Claim 1's "logic element" limitation alternatively recites generating "gated column access strobe (CAS) signals . . . in response at least in part to (i) row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal." PO Response 3. Amidi's CPLD 604 does not teach or suggest generating a CAS signal. *See* Amidi, Fig. 6A. Instead, CAS signals enter (e.g., CAS) and exit (e.g., rCAS) register 608. *See id.* Granted, Amidi's register 608 receives row address signals (e.g., Add[n-1:0]), bank address signals (e.g., BA[1:0]), and PLL signals (e.g., CLK0, CLK0_N). *See id.* ¶ 50, Fig. 6A. Yet, Amidi does not describe how the rCAS signal is generated. *See id.* Moreover, Amidi does not teach or suggest register 608 receiving chip-select signals (i.e., signal (iv) in claim 1) or operates as a logic element to generate gated CAS signals as recited. *See id.* As such, Amidi does not teach and suggest the "logic element" limitation in claim 1.

Additionally, Dell 2 does not teach or suggest the above missing feature. As explained above, Dell 2 teaches or suggests storing a bank address signal for use with a logic element (e.g., ASIC 24) during CAS time. Dell 2, 8:29–40, 9:32–34. Yet, there is no discussion of generating a CAS signal in response to signals (i) through (iv) as recited in claim 1. In particular, Dell 2 fails to teach or suggest generating a CAS signal in response to a chip-select signal (i.e., signal (iii)). Nor do we find Dr. Wang's testimony persuasive in teaching or suggesting generating a CAS signal in response to a chip-select signal. *See* Dec. 80–81 (citing 3d Wang Decl. ¶¶ 10–16). On the record, we therefore determine Amidi and Dell 2 collectively do not teach or suggest sufficiently to one skilled in the art the "logic element" limitation generating CAS signals in response to both a row address

signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Lastly, Requester 1 points out Dr. Sechen's statement in paragraph 26 regarding "the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers." 2d Supp. Sechen Decl. ¶ 26, *cited in* R1 Comments 11. We agree with Requester 1 that claim 1's "logic element" limitation as currently recited requires the logic element to receive both a row address signal *and* bank address signals. *See* PO Response 3. From this perspective, Dr. Sechen's statement is confusing. *See* R1 Comments 11. Yet, when focusing on the recitation "the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element" in claim 1 (PO Response 3), Dr. Sechen's testimony is consistent with claim 1's recitation requiring the logic element to receive a separate or different row/column address signal from the row/column address signals entering the register. *See* 2d Supp. Sechen Decl. ¶ 26.

Independent claims 15, 28, and 39 each recite a similar "logic element" limitation to claim 1, which generates gated CAS signals or chip-select signals in response to signals (i) through (iv), including both a row address signal and bank address signals. PO Response 11, 18, 23–24. For the above reasons, we determine Amidi's and Dell 2's teachings are inadequate to teach or suggest the "logic element" limitation in these claims.

Upon reconsideration of the record, we withdraw the rejection of claims 1, 15, 28, and 39 and dependent claims 3, 4, 6, 8, 10–14, 18–20, 22, 24, 27, 29, 31,

32, 34–38, 40, 41, 43, 45–50, 120, 122, and 132–136, which variously depend from claims 1, 15, 28, and 39, based on Amidi and Dell 2.

B. Amidi, Dell 2, and JEDEC 21C

The rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C was newly proposed by Requester 1 in its comments. R1 Comments 12–77. The Examiner adopted this proposed rejection. Ex. Deter. 11. Specifically, concerning the "logic element" limitation found in independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58, Requester 1 proposes a similar mapping and reasoning for combining Amidi with Dell 2 to teach or suggest this recitation. *See, e.g.,* R1 Comments 23. Requester 1 adds JEDEC 21-C teaches or suggests transmitting PLL clock signals to a CPLD and, and when combined with Amidi, generating its output control signals (e.g., rank-selecting or chip-select signals) in response to a PLL signal for clocking additional devices on a DIMM. *See* R1 Comments 22 (citing JEDEC 21-C, pp. 38–43), 23. In essence, based on JEDEC 21-C's teaching, Requester 1 states one skilled in the art would have known or recognized modifying Amidi so that the clock signals comes Amidi's PLL 606 (e.g., PLL clock signals) rather than memory connector 602 for clocking DIMM devices. *See id.* at 22–23. This modification, in turn, generates chip-select or rank-selecting signals in response to a PLL clock (i.e., signal (iv)) as recited. *See id.*

Yet, JEDEC 21-C's teaching is not relied upon and does not cure the above-noted deficiencies in Amidi and Dell 2—namely the "logic element" limitation generates gated CAS, chip-select or rank-selecting signals in response to

both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv). We refer above for more details.

Accordingly, we withdraw the adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C.

C. Amidi and Dell 184 (Ground 20)

In our May 31, 2016 Decision, claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 (canceled claims omitted) are rejected under 35 U.S.C. § 103 based on Amidi and Dell 184. Dec. 91–93. Independent claims 52, 67, 77, 82, and 87 include similar recitations to the "logic element" limitation in claim 1 that generates rank-selecting or chip-select signals in response to signals (i) through (iv). *Compare* PO Response 27, 33, 36, 38, and 41 *with id.* at 3. Notably, claims 52, 57, 77, 82, and 87 exclude the alternative recitation of generating a gated CAS signal. *Id.* at 27, 33, 36, 38, and 41.

Our rationale for rejecting these claims based on Amidi and Dell 184 was similar to that proposed for Amidi and Dell 2. Specifically, we noted in the opinion

> The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48-3:5, claim 1, a[n]d Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the

> desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal . . . .

Id. at 92–93.

Similar to that noted above when addressing Dell 2, Dell 184 in combination with Amidi may provide a reason why bank address signals may be received by a CPLD, but does not sufficiently address why one skilled in the art would have specifically recognized Amidi's CPLD (e.g., a logic element as recited in claim 52) generates *chip-select* or *rank-selecting* signals in response to signals (i)–(iv) as recited in claims 52, 67, 77, 82, and 87. We refer above for more details.

Requester 2 asserts Patent Owner provided no argument related to the patentability of the claims rejected based on Ground 20 and relied upon the arguments presented for Micron and Amidi. *See* R2 Comments 10 (stating "Patent Owner did not provide any individual analysis concerning the patentability of those claims in view of this rejection, but rather relied on its analysis for the rejections under Micron and Amidi."). We disagree.

Patent Owner states "[t]hese amendments [to the claims presented after the previous Decision] distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV." PO Response 56. In "Section IV" of the declaration, Dr. Sechen discusses the similarities between the teachings of Dell 184 and Dell 2 and further articulates how Dell 184 does not use bank address inputs for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 38, 40–42. As such, when stating "as discussed above" (PO Response 56), Patent Owner was referring to the rejection of Amidi and Dell 2 and not Micron and Amidi as argued.

Accordingly, we withdraw the rejection of claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184.

D. Micron and Amidi (Ground 13)

In our previous Decision, we determined claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 (canceled claims omitted) were obvious over Micron and Amidi. Dec. 93–99. For this rejection, Patent Owner reasserts Amidi does not use both bank address signals and row address signal for rank multiplication or for generating chip-select signals/CAS signals. PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30). As to whether one skilled in the art would be motivated to use bank address signals for proper operation of chip select signals, Patent Owner contends "this is a conclusion of fact and not an indication of what a POSITA[17] would recognize." *Id.* at 55 (citing 2d Supp. Sechen Decl. ¶¶ 32–33); *see also id.* at 55–56 (citing 2d Supp. Sechen Decl. ¶¶ 34–35). Patent Owner argues combining Micron and Amidi to arrive at the claimed invention as amended would not be obvious to one skilled in the art. *Id.* at 56. For reasons discussed below, we are persuaded Micron and Amidi do not teach or suggest the newly recited "logic element" limitation in claim 1 or similar independent claims.

At the outset, we address Patent Owner's argument that Dr. Kozyrakis's testimony represents how an expert—not an ordinarily skilled artisan—would have understood Amidi and that Amidi, which does not teach using bank signals to generate chip-select or CAS signals for rank expansion, is representative of what one skilled in the art would have understood. *Id.* at 54–55 (citing 2d Supp. Sechen Decl. ¶¶ 31–32). We agree with Requester 3 that Dr. Kozyrakis's testimony is

[17] "POSITA" stands for a person of ordinary skill in the art.

from the point of view of what an ordinarily skilled artisan would have known or recognized. *See* R3 Comments 12 (citing Kozyrakis Decl. ¶ 8, 2d Kozyrakis Decl. ¶¶ 12–14, 3d Kozyrakis Decl. ¶¶ 9–11, 4th Kozyrakis Decl. ¶¶ 12–14). For example, Dr. Kozyrakis testifies that one of ordinary skill in the art (e.g., two or more years of professional experience in memory design)[18] would have an understanding of "the latest memory devices," including DDR, DDR-2, and DDR-3 devices, and "the number of rows, columns, banks, and input/output bits of each device." 2d Kozyrakis Decl. ¶ 14, 3d Kozyrakis Decl. ¶ 11, and 4th Kozyrakis Decl. ¶ 14. On the other hand, we also agree with Patent Owner that "Amidi is representative evidence of what a POSITA would understand." PO Response 55; *see also* Dec. 27 (stating Amidi "reflects the appropriate skill level at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).").

Next, the amendments to independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58 have been made to include the "logic element" limitation that generates gated CAS, chip-select, or rank-selecting signals in response to four enumerated signals, signals (i) through (iv). *See* PO Response 2–3, 10–11, 17–18, 22–27, and 29–41. As stated above when addressing Ground 5, Amidi does not teach to an ordinarily skilled artisan using bank address signals to generate CAS signals or chip-select signals. *See also* Dec. 95 (stating "these

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[18] Our previous Decision established that one of ordinary skill in the art "is a person with (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline and (2) at least two years of experience in designing computer memory systems. This ordinarily skilled artisan would also have familiarity with and understanding of (1) JEDEC standards related to memory devices and modules, such as DDR SDRAM devices and DIMMs, and (2) the latest DRAM memory devices in the market." Dec. 26–27.

passages in Amidi do not discuss using a *bank* address bit to generate the chip-select signals.") (referring to Amidi ¶¶ 43–44, 52). However, we previously noted "Amidi suggests other types of memory devices or densities can be used to build [its] four rank memory module." Dec. 42 (citing Amidi ¶ 71); *see also* Amidi ¶¶ 10–12, *cited in* Dec. 96. We therefore turned to what "an ordinarily skilled artisan would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." Dec. 95.

In referring to "our previous discussion," (*id.*), we stated

> Amidi, when accounting for inferences and creative steps that a person of ordinary skill in the art would have employed, at least suggests generating a chip-select signal in response in part to a bank address signal. For example, Requester 3's *second case* of using a spare bank address signal to generate the proper chip-select signals for rank multiplication as taught by Amidi is similar to our previous discussion of the collective teachings suggest a CPLD receiving a bank address signal.

Id. at 94–95. For example, Dr. Kozyrakis stated one skilled in the art would have recognized different generation of DDRs (e.g., DDR-1, DDR-2, and DDR-3) and that some DDR-2 devices have an extra bank address field (e.g., 3 bits rather than the conventional 2 bits). *Id.* at 61–62 (citing Kozyrakis Decl. ¶ 26); *see also* 3d Kozyrakis Decl. ¶¶ 22–25. We then concluded this provides evidence that one skilled in the art would have recognized or known a bank address signal is free in certain DDR devices to assist in creating the desired rank expansion for certain memory modules. *See id.* at 62; *see id.* at 65–66 and 98.

In particular, we stated:

> [L]ike Amidi's teaching of using an extra row/column address bit for generating the proper chip-select signals (e.g., rank expansion) for

> emulating a two rank memory module (Amidi ¶¶ 51, 59), Dr. Kozyrakis provides a reason with some rational underpinning that an ordinary skilled artisan would have used other known, extra address bits (e.g., the extra bank address in more recent DDR devices) to create the desired rank expansion in Amidi by directing such extra signals to Amidi' s CPLD.

Id. at 62. We maintain our position that the record provides a reason with a rational underpinning to use *a* free signal—whether a row address or a bank address signal—to achieve desired rank expansion. Despite Patent Owner asserting this "second case" no longer applies "to the amended claims" (PO Response 54), neither Patent Owner nor Dr. Sechen's testimony (2d Supp. Sechen Decl. ¶ 29) sufficiently explains why this scenario no longer pertains to the amended claims or why bank signals cannot be used by both the registers and a logic element. *See* R3 Comments 10.

Additionally, in the previous Decision, we noted Amidi uses an extra row or column address signal as an input to the CPLD to generate chip-select signals and uses a column address signal (e.g., A11) for multiple purposes. Dec. 63–64 (citing Amidi ¶¶ 50–52, 57–60, Figs. 6A–B). Based on Amidi's teaching, we concluded an ordinary skilled artisan having two years of experience in logic circuit design would have recognized to use address signals in an unconventional manner and for multiple purposes. We additionally found Requester 3 provides adequate evidence that one skilled in the art would have recognized using bank address signals in a manner similar to the row and column address signals, some of which are received by Amidi's CPLD. *Id.* at 64, 66. Yet, the evidence of record does not teach or suggest generating the specifically recited chip-select signals using more than one bank address signal and, more particularly, both bank address

signal*s* (i.e., signals (ii)) and a row address signal (i.e., signal (i)) as well as signals (iii) and (iv) claimed in claim 1.

Requester 3 offers yet another reason for a logic element to generate chip-select signals in response to both multiple bank address signals and a row address signal. *See* Dec. 96–97 (citing R3 App. Br. 7–10, R3 Reb. Br. 2, 4, 3d Kozyrakis Decl. ¶¶ 17–19, 4th Kozyrakis Decl. ¶¶ 15–25, and Amidi ¶ 61). In particular, Requester 3 stated previously (*see* R3 App. Br. 10) and now (*see* R3 Comments 13) "[b]ecause the extra row address bit [used during row address time] is unavailable at column address time, the rank-multiplying module must store information from row address time for use during column access time." R3 Comments 13 (citing 3d Kozyrakis Decl. ¶ 19). According to Requester 3, "[i]nput bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals at column address time. Kozyrakis Decl. III ¶ 19." R3 Comments 13; *see also* R3 App. Br. 7. Requester 3 thus asserts chip-select signals are generated in response to both a row address signal and bank address signals

> because the input bank address signals are used to select the previously stored "highest [row] address number Add(n)" needed to generate the chip-select signals matching those generated at RAS time. In other words, the CPLD 604 would generate chip-select signals based on the stored row address bit, which is selected based on the input bank address signals from the memory controller.

R3 App. Br. 10, *quoted in* Dec. 97.

Turning to Amidi, this reference teaches CPLD 410's circuitry for row address decoding and column address decoding (e.g., row address time and column address time) differs. Amidi ¶ 61. Amidi states the "Row

address" cycle and "the Column address" cycle need to be provided with "the proper control and command signals" but fails to provide any specifics related to which control and command signals are provided during these cycles. *Id.* Nor does Amidi show or suggests bank address signals entering CPLD 604 during row address or column address decoding. *See id.*, Figs. 6A–B; *see also* PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30).

Concerning row and column address time, Dr. Kozyrakis states an ordinary artisan would have known of alternative scenarios from Amidi where the logic element can decode or pre-process the one row address bit, store the resulting signals from decoding or pre-processing, and then use the stored, resulting signals during column access operations "to generate chip-select signals or the bank address field." 2d Kozyrakis Decl. ¶ 18(d)(ii); *see also id.* ¶ 33. In this scenario, decoded or pre-processed signals—not bank address signals—are used during column access time to generate chip-select signals. Dr. Kozyrakis further states "bank address are not always necessary in order to determine the output control signals for the lower density memory devices," such as in Amidi. 2d Kozyrakis Decl. ¶ 23. As such, Dr. Kozyrakis's testimony conflicts with Requester 3's position that bank address signals *are necessary* (R3 Comments 13) to generate the chip-select signals during column access time.

Nevertheless, Dr. Kozyrakis also asserts an "obvious way to know which of the two banks has the proper row open" during subsequent CAS commands is to store the address bit (e.g., A_{13}) and to reuse the stored address bit to identify the correct pair of banks (e.g., reuse as a bank address signal). *See* 3d Kozyrakis Decl. ¶¶ 18–19. Notably, Dr. Kozyrakis does not

discuss how the stored address bits are located during subsequent CAS commands (*see id.*), such as by using bank address signals as Requester 3 asserts (R3 Comments 13).

To elaborate, Dr. Kozyrakis testifies that a memory module's controller must identify which bank should receive the CAS command using bank address and chip-select signals. 3d Kozyrakis Decl. ¶¶ 17–18. Dr. Kozyrakis also states the incoming bank address and chip-select signals from a memory controller are not sufficient for certain rank-multiplying modules. *Id.* ¶ 18 (discussing "the case where the originally specified module uses two ranks of 512Mbit DDR2 devices [having four banks] and the rank-multiplying module uses four ranks of 256Mbit DDR2 devices [having four banks]."). Specifically, during a RAS command to a bank in a 512Mb device, Dr. Kozyrakis states a rank-multiplying module designer would use bank address and chip-select signals to identify a bank pair from eight banks and would use a free address bit (e.g., A_{13}) to identify which of the two banks in the bank pair will receive a command. *Id.* ¶ 19.

During a subsequent CAS command, Dr. Kozyrakis further states the memory controller does not provide the free address (e.g., A_{13}) bit to identify the correct bank in the bank pair. *Id.* Thus, Dr. Kozyrakis states an obvious way to identify the correct bank in a pair with the proper row open is to store the address bit of the last RAS command (e.g., A_{13}) and to reuse the stored address bit. *Id.* However, unlike Requester 3's assertion that bank address signals are used to identify this stored address bit (R3 Comments 13), Dr. Kozyrakis does not additionally testify the incoming bank address signals are used to identify the stored address bit. 3d Kozyrakis Decl. ¶ 19.

Instead, Dr. Kozyrakis states "the module must have a total of 8 bits of storage for A_{13} address bits" without discussing how the proper address bit is identified. *Id.*

Dr. Kozyrakis's testimony in his fourth declaration also cited by Requester 3 (R3 Comments 13) does not further explain or address how stored address bits are identified—namely, whether or not using bank address signals are used. *See, e.g.*, 4th Kozyrakis Decl. ¶¶ 15–25, *cited in* R3 Comments 13. Similarly, Dr. Bagherzadeh also states storing the extra address bit is "a standard feature in transparent memory modules like the embodiments disclosed in Amidi" and the circuit "will be unable to identify the correct chip to access during the column access procedure" if the extra bit is not stored. 2d Bagherzadeh Decl. ¶ 22. But, once again, Dr. Bagherzadeh does not explain how the stored address bit is later identified.

Granted, Dr. Kozyrakis and Dr. Wang point to references in asserting one skilled in the art would have known to store some address bits for each bank in a logic device and use them later during column commands. 4th Kozyrakis Decl. ¶ 24 (citing Olarig); *see* 3d Wang Decl. ¶ 10 (citing Dell 2). Nevertheless, Olarig and Dell 2 form no part of this rejection based on Micron and Amidi and thus are not persuasive. Moreover, these references do not teach or suggest using bank address signals later to identify the stored bits.

Moreover, to the extent Dr. Kozyrakis's testimony does suggest bank address signals are used to identify the stored bits, this position clashes with his earlier testimony stating

> bank address signals must be used as one of the inputs for the calculation of the output chip-select signals *only if* the number of

> banks in the memory devices used in the lower cost memory module is *smaller* than the number of banks in the memory devices in the originally specified module. In all other cases, the bank address signals can be simply clocked through the logic element . . . without further processing.

2d Kozyrakis Decl. ¶ 23 (italics added). In the example provided in the third declaration (3d Kozyrakis Decl. ¶¶ 18–19), the bank number of the lower cost memory module's memory devices (e.g., 256Mb devices having four banks) is not smaller than the originally specified module's memory devices (e.g., 512Mb devices also with four banks), implying that bank address signals will only be clocked through the logic element. *See id.* Additionally, Dr. Kozyrakis states the bank address signals "must be used as *one* of the inputs for the calculation of the output chip-select signals" (2d Kozyrakis Decl. ¶ 23 (italics added)) when the bank number in the lower cost memory module is smaller than the bank number of the originally specified module, suggesting at most one bank address signal—instead of bank address signals (i.e., signals (ii))—is used.

Thus, Requester 3's assertions that Amidi's "CPLD 604 would generate chip-select signals based on the stored row address bit, *which is selected based on the input bank address signals from the memory controller*" (R3 App. Br. 10) (emphasis added) is not corroborated adequately with Dr. Kozyrakis's testimony. Likewise, Requester 3's conclusion that it would have been obvious to an ordinarily skilled artisan to generate chip-select signals in response to both a row address signal and "input bank address signals during column address time, because the input bank address signals must be used to identify the stored row address bit

required to generate the chip select signals" (*see* R3 Comments 13; *see also* R3 App. Br. 7) is not corroborated sufficiently by Dr. Kozyrakis.

Additionally, Dr. Sechen provides countering evidence and arrives at the opposite conclusion of Requester 3. 2d Supp. Sechen Decl. ¶¶ 22 (citing Sechen Decl. ¶ 23, 2d Sechen Decl. ¶¶ 14–15), 29 (citing "Section II"). Specifically, Patent Owner and Dr. Sechen focus on Amidi and assert this reference demonstrates what one skilled in the art would have recognized. PO Response 55. Patent Owner and Dr. Sechen state Amidi provides no recognition to one of ordinary skill that bank address signals are necessary for generating chip-select signals. 2d Supp. Sechen Decl. ¶¶ 33, 35; PO Response 54–55. Dr. Sechen further states Amidi does not recognize generating chip-select signals using both the bank address signals and a row address signal as recited in claim 1 for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 29, 31, 32; *see also* PO Response 55. Dr. Sechen testifies additionally Amidi and Micron do not teach using bank address signals to generate rank or chip-select signals and that using the bank address signals in this manner would not have been known by one of ordinary skill based on Micron and Amidi. Sechen Decl. ¶¶ 35, 37. Patent Owner and Dr. Sechen argue one skilled in the art "would conclude that Amidi is operative without bank address signals for generating control signals." 2d Supp. Sechen Decl. ¶ 33; *see also* PO Response 55.

As previously noted, we agree that Amidi provides evidence of what one skilled in the art would have known or recognized at the time of the invention. *See Okajima*, 261 F.3d at 1355. As such, we agree with Dr. Sechen that one skilled in the art "would conclude that Amidi is operative without bank address signals for

generating control signals," and thus a memory module's logic element (e.g., Amidi's CPLD) can generate chip-select signals without using bank address signals. *See* 2d Supp. Sechen Decl. ¶ 33. Although an obviousness "analysis need not seek out precise teachings" and we further consider an ordinarily skilled artisan's background knowledge (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)), Dr. Kozyrakis's testimony and Requester 3's articulated reason that bank address signals are known to be used to identify the row address signal, which in turn is used generate chip-select signals, lacks sufficient corroborating evidence to provide a rational underpinning to support an obviousness conclusion. *See id.*

Lastly, Requester 3 notes that claims 52, 123, and 129 recite similar limitations to claim 1 (excluded a PLL clock signal (i.e., signal (iv)) and were addressed in our previous Decision. R3 Comments 8–9. We acknowledge claims 52, 128, and 129 were previously rejected based on Micron and Amidi. Dec. 93–99. However, the specific limitations found in claims 52, 128, and 129 similar to the "logic element" limitation in claim 1 as now amended were not disputed in Requester 3's brief. For example, regarding claim 52, Requester 3's arguments referred back to claim 1 as previously recited (*see* Dec. 98 (citing R3 App. Br. 12 (stating "[a]s discussed above, it would have been obvious for the chip-select signals generated as CAS time to be generated based on *an* input bank address") (italics added))), which did not include the "logic element" limitation found in claim 1 as now amended.

Upon reconsideration of claim 1 as now amended, we withdraw our conclusion of obviousness for these claims based on Micron and Amidi. We also withdraw the remarks made in our previous Decision concerning one skilled in the art would have recognized using bank address signal*s* for generating chip-select

signals (*see* Dec. 96–97), in view of the above discussion. Weighing all the evidence in the record, we determine one skilled in the art would not have recognized using a known logic element, such as Amidi's, to generate chip-select signals in response to a row address signal (i.e., signal (i)), multiple bank address signals (i.e., signals (ii)), a chip-select signal (i.e., signal (iii), and a PLL clock signal (i.e., signal (iv)) as recited in claim 1.

Regarding the logic element alternatively generating gated CAS signals in response to signals (i) through (iv) as recited in claim 1 (PO Response 3), there is insufficient evidence to support such CAS signals are generated in response at least in part to these signals. *See* R3 Comments 11–13 (focusing on generating chip-select signals); *see also* 3d Kozyrakis Decl. ¶¶ 16–19, 22–25 (discussing receiving a CAS command and generating chip-select signals) and 4th Kozyrakis Decl. ¶¶ 22–24 (same). As discussed above, Amidi's CPLD 604 does not teach or suggest generating a CAS signal but rather a CAS signal entering (e.g., CAS) and exiting (e.g., rCAS) register 608. *See* Amidi, Fig. 6A. Amidi also does not (a) describe how the rCAS signal is generated or (b) teach or suggest chip-select signals entering register 608. *See id.* ¶ 50, Fig. 6A. Micron similarly does not disclose or teach how gated CAS signals are generated. *See* Micron 5–8.

For the above reasons, we withdraw our rejection of claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi.

E. Micron, Amidi, and Olarig (Ground 21)

Above, we stated Requester 3 provided insufficient evidence to support the assertion that bank address signals are necessary for generating

gated CAS/chip-select signals or that one skilled in the art would have recognized using both a row address signal and bank address signals as well as signals (iii) and (iv) for this purpose. Unlike Ground 20, Olarig is also being relied upon in Ground 21. Thus, Dr. Kozyrakis's testimony concerning storing some address bits for each bank in a logic device and using them later during column commands illustrates storing and reusing an address bit for a later operation is known to an ordinary skilled artisan. 4th Kozyrakis Decl. ¶ 24 (citing Olarig). But, this teaching does not further illustrate using bank address signals to identify the stored row address bit as Requester 3 asserts. *See* R3 Comments 13.

> Nevertheless, as indicated in our previous Decision,
>
> Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49-51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.* Granted, there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited. *Id.* But, we agree with Requester 3 that this teaching in Olarig illustrates using bank address signals to generate other control signals was known. *See* R3 App. Br. 18-19.

Id. at 100. We then concluded "Olarig teaches combining address signals, including a bank address signal, to generate another control signal, and artisans armed with Olarig's and Amidi's teachings and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as chip-select signals." *Id.* at 101.

This analysis indicates an ordinary artisan would have recognized to combine address signals with *a* bank address signal to generate control signals. But, even this teaching falls short of suggesting generating a control

signal, such as a chip-select signal, in response to both at least one row address signal (e.g., recited signal (i)) and bank address *signals* (i.e., signals (ii)) recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 46–48. Granted, we also concluded "when combined with Amidi' s teachings, the collective teachings suggest that an ordinarily skilled artisan would have recognized generating a chip-select signal in response at least in part to bank address signal*s*." *Id.* at 100–101 (italics added). In light of the record before us now, we no longer conclude Amidi, Dell 2, and Olarig collectively teach or suggest combining multiple bank address signals with a row address signal as well as signals (iii) and (iv) to generate chip-select (or gated CAS signals for that matter).

Requester 3 asserts Patent Owner relies on "Section IV," which is directed to the rejection based on Micron and Amidi, and does not address Olarig. R3 Comments 13. For this reason, Requester 3 argues Patent Owner fails to show the claims rejected based on Micron, Amidi, and Olarig are unobvious. *Id.*

Patent Owner refers to its previous discussion when address the rejection based on Micron, Amidi, and Olarig. PO Response 56–57. As noted above, based on the record, we are persuaded that Micron and Amidi do not sufficiently demonstrate the "logic element" limitation found in the independent claims as now amended. We refer above for more analysis. Patent Owner also refers to "Second Supp. Sechen Decl. Section V" (*id.* at 57), which discusses Olarig. *See* 2d Supp. Sechen Decl. ¶¶ 45, 48–52. We thus disagree with Requester 3 that Patent Owner does not address Olarig in its remarks.

In "Section V" of the declaration, Dr. Sechen notes our previous Decision stating Olarig teaches combining a bank address signal with a column address bit to generate an output signal. 2d Supp. Sechen Decl. ¶ 45. Dr. Sechen further asserts that one skilled in the art would not reach the conclusion that Amidi and Olarig teach the claims as now amended. *Id.* ¶¶ 46–48. Although we disagree with Dr. Sechen that one skilled in the art would not recognized using a bank address signal to generate chip-select signals (*see id.*) for reasons previously stated, we agree that Amidi and Olarig alone or in combination with Micron do not suggest generating gated CAS, chip-select, or rank-selecting signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv) as now recited in claim 1. Requester 3 provides no rebuttal to Dr. Sechen's testimony. *See* R3 Comments 13.

For the above reasons, we withdraw our rejection of claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig.

F. Proposed Rejections based on Micron, Amidi, and Additional References

In the earlier Decision, we did not reach the proposed rejections set forth in Ground 19 (Micron, Amidi, Dell 2, and JEDEC 79C) and Ground 22 (Micron, Amidi, Olarig, and Memory Explained[19]). Dec. 101.[20] Based on the amendments

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[19] *HP Printer Memory Explained* 1-7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained).

[20] We mistakenly included Grounds 7 and 20 in Section (III)(4)'s heading. Dec. 101. Ground 7 was addressed in the previous Decision, indicating that the Examiner determined there was no substantial new question (SNQ) of patentability for this proposed rejection. *Id.* at 83–84. Further, as discussed above in Section (III)(C), Ground 20 was also addressed. *Id.* at 90–93.

to claims 1, 15, 58, 67, 77, 82, and 87 and our withdrawal of the other grounds, we now consider the Examiner's decision not to adopt these proposed rejections.

Specifically, the Examiner did not adopt the following proposed rejections:

Reference(s)	Basis	Claims (canceled claims omitted)	
Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)	§ 103	1, 15, 28, 39, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	RAN 14–15; R3 App. Br. 13
Micron, Amidi, Olarig, and Memory Explained (Ground 22)	§ 103(a)	56	RAN 15

1. Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)

Above, we addressed the rejection of Micron and Amidi in Section (III)(D), concluding that one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as now recited in claims 1, 15, 58, 67, 77, 82, and 87. We additionally addressed rejections based on Amidi and Dell 2 (Section (III)(A) and Amidi, Dell 2, and JEDEC 21-C (Section (III)(B)), also concluding one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals, chip-select or rank-selecting signals in response to signals (i)–(iv) as now recited. We refer above for more details.

As discussed in the context of the rejection of Amidi and Dell 2 (Ground 5), Dell 2 does not teach or suggest the missing feature of using both signal (i) and signals (ii) to generate gated CAS, chip-select, or rank-selecting signals as now recited in claims 1, 15, 52, 58, 67, 77, 82, and 87. We refer above for more details.

Regarding JEDEC 79C, Requester 3 does not explain how this reference is being relied upon in its Appeal Brief. *See* R3 App. Br. 13–17. Moreover, the cited comments, submitted August 29, 2011, in the Appeal Brief do not address JEDEC 79C. *Id.* at 14 (citing pages 18 and 19). As for Appendix L also cited in the Appeal Brief, (*id.*), the proposed rejection discusses how JEDEC 79C teaches a read operation reads from the row selected by the preceding activate command on the same bank. Requester 3's August 29, 2011 Comments, App'x L, p. 1 (addressing claim 52). Yet, this teachings do not suggest the missing feature of generating gated CAS signals or chip-select signals in response to both a row address signal (i.e., recited signal (i)) and bank address signals (i.e., recited signals (ii)). *See id.*, App'x L, pp. 1–2. We thus determine Requester 3 has not sufficiently demonstrated how JEDEC 79C teaches or suggests the claimed features missing from Micron, Amidi, and Dell 2.

Accordingly, we determine the Examiner has not erred in not adopting the proposed rejection of claims 1, 15, 28, 39, 52, 54, 56, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 (canceled claims omitted) based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19).

2. Micron, Amidi, Olarig, and Memory Explained (Ground 22)

Above, we addressed the rejection of Micron, Amidi, and Olarig in Section (III)(E), concluding that one skilled in the art would have not recognized based on

the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as recited in claims 1, 15, 28, 39, 52, and 58.

As for Memory Explained, the Examiner stated and we agree that this reference, even when combined with Micron, Amidi, and Olarig, does not teach or suggest generating CAS or chip-select signals in response to bank address signals (i.e., signals (ii)) as well as recited signals (i), (iii), and (iv). RAN 58–69. Requester 3 does not rebut this determination. R3 App. Br. 19 (asserting Micron, Amidi, and Olarig teach these features). In particular, Requester 3 turns to Memory Explained to teach the features recited in dependent claim 56, not the features in independent claim 52. *See* Requester 3's February 13, 2013 Comments 24–25, App'x S.

For the above reasons, we determine the Examiner has not erred in not adopting the proposed rejection of claim 56 (as well as claims 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131)[21] based on Micron, Amidi, Olarig, and Memory Explained (Ground 22).

V. CONCLUSIONS

We withdraw the following rejections maintained or adopted by the Examiner.

(1) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5).

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[21] Despite including only claim 56 in our previous Decision (Dec. 69), Requester 3 appealed the Examiner not adopting the rejection of claim 56 as well as the remaining claims listed above. R3 App. Br. 19–22.

(2) Claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Amidi and 184 (Ground 20).

(3) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Amidi, Dell 2, and JEDEC 21-C.

(4) Claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Micron and Amidi (Ground 13).

(5) Claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Micron, Amidi, and Olarig (Ground 21).

We further affirm the Examiner's decision not to adopt the rejection of certain claims based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19) or Micron, Amidi, Olarig, and Memory Explained (Ground 22), previously not reached.

Based on our previous Decision, we note the following rejections are affirmed.

(1) Claim 9 and 33 is rejected under 35 U.S.C. § 102 based on Amidi. Dec. 11, 13, 23.

(2) Claims 2, 5, 7, 9, 21, 23, 30, 33, 57, and 119 are rejected under 35 U.S.C. § 103 based on (a) Amidi or (b) Amidi and JEDEC. Dec. 12–13, 39, 57.

(3) Claims 2, 5, 7, 9, 21, 23, 26, 30, and 33 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 12–13, 43, 60.

(4) Claims 7, 9, 21, 26, 33, and 57 are rejected under 35 U.S.C. § 103 based on Micron and Amidi. Dec. 12–13, 66–67.

(5) Claim 9 is rejected based on (a) Dell 1[22] and JEDEC under 35 U.S.C. § 103 (RAN 13, 36–39) (Ground 9), (b) Wong[23] and JEDEC under 35 U.S.C. § 103 (RAN 13, 41–43) (Ground 11), and (c) Micron and Connolly[24] under 35 U.S.C. § 103 (RAN 13, 44–47) (Ground 12). Dec. 12–13.

We also note the Examiner's decision not to adopt the proposed rejection of claims 16 and 17 based on Amidi and Dell 2 remains affirmed and we do not reach the propriety of the non-adopted rejection of claim 119 under Ground 5. Dec. 82–83.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

37 C.F.R. § 41.77(f)

[22] U.S. Patent No. 5,926,827 (issued July 20, 1999) (Dell 1).
[23] U.S. Patent No. 6,414,868 (issued July 2, 2002) (Wong).
[24] U.S. Patent No. 5,745,914 (issued April 28, 1998) (Connolly).

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